TIERED BUILT-IN SELF-TEST (BIST) ARCHITECTURE FOR TESTING DISTRIBUTED MEMORY MODULES

ABSTRACT

A distributed, hierarchical built-in self-test (BIST) architecture for testing the operation of one or more memory modules is described. As described, the architecture includes three tiers of abstraction: a centralized BIST controller, a set of sequencers, and a set of memory interfaces coupled to memory modules. The BIST controller stores a set of commands that generically define an algorithm for testing the memory modules without regard to the physical characteristics or timing requirements of the memory modules. The sequencers receive the commands and generate sequences of memory operations in accordance with the timing requirements of the various memory modules. The memory interfaces apply the memory operations to the memory module in accordance with physical characteristics of the memory module, e.g., by translating address and data signals based on the row-column arrangement of the memory modules to achieve bit patterns described by the commands.